

Bangladesh University of Engineering and Technology

Dept. of Electrical and Electronic Engineering

EEE 303: Digital Electronics

Syllabus:

Introduction to number systems and codes. Analysis and synthesis of digital logic circuits: Basic logic functions, Boolean algebra, combinational logic design, minimization of combinational logic. MOSFET Digital circuits: NMOS inverter, CMOS inverter, CMOS logic circuits, Clocked CMOS logic circuits, transmission gates, sequential logic circuits,

Memories: classification and architecture, RAM memory cells, Read only memory, data converters, BJT digital circuits: ECL, TTL, STTL, BiCMOS, Design application A static ECL gate.

Modular combinational circuit design: pass transistor, pass gates, multiplexer, demultiplexer and their implementation in CMOS, decoder, encoder, comparators, binary arithmetic elements and ALU design.

Sequential circuits: different types of latches, flip-flops and their design using ASM approach, timing analysis and power optimization of sequential circuits. Modular sequential logic circuit design: shift registers, counters and their applications. State Machine Design.

Asynchronous and synchronous sequential circuits.

Topics covered:

Text Book:

Fundamentals of Digital Logic with Verilog Design, 3rd ed, - Stephen Brown, Zvonko Vranesic.

Chapter 2: Introduction to Logic Circuits

2.1 Variables and Functions

2.2 Inversion

2.3 Truth Table

2.4 Logic Gates and Networks

2.4.1 Analysis of a Logic Network

2.5 Boolean Algebra

2.5.2 Notation and Terminology

2.5.3 Precedence of Operations

2.6 Synthesis Using NAD, OR, and NOT Gates

2.6.1 Sum-of-Products and Product-of-Sums Forms

2.7 NAND and NOR Logic Networks

2.8 Design Examples

2.8.1 Three-Way Light Control

2.8.2 Multiplexer Circuit

2.11 Minimization and Karnaugh Maps

2.12 Strategy for minimization

2.12.1 Terminology

2.13 Minimization of Product-of-Sums Forms

2.14 Incompletely Specified Functions

2.15 Multiple-Output Circuits

Chapter 3: Number Representation and Arithmetic Circuits

- 3.1 Positional Number Representation
 - 3.1.1 Unsigned Integers
 - 3.1.2 Octal and Hexadecimal Representations
- 3.2 Addition of Unsigned Numbers
 - 3.2.1 Decomposed Full-Adder
 - 3.2.2 Ripple-Carry Adder
 - 3.2.3 Design Example
- 3.3 Signed Numbers
 - 3.3.1 Negative Numbers
 - 3.3.2 Addition and Subtraction
 - 3.3.3 Adder and Subtractor Unit
 - 3.3.5 Arithmetic Overflow
 - 3.3.6 Performance Issues
- 3.4 Fast Adders
 - 3.4.1 Carry-Lookahead Adder
- 3.7 Other Number Representations
 - 3.7.1 Fixed-Point Numbers
 - 3.7.2 Floating-Point Numbers
 - 3.7.3 Binary-Coded-Decimal Representation

Chapter 4: Combinational-Circuit Building Blocks

- 4.1 Multiplexers
 - 4.1.1 Synthesis of Logic Functions Using Multiplexers
 - 4.1.2 Multiplexer Synthesis Using Shannon's Expansion
- 4.2 Decoders
 - 4.2.1 Demultiplexers
- 4.3 Encoders
 - 4.3.1 Binary Encoders
 - 4.3.2 Priority Encoders
- 4.4 Code Converters
- 4.5 Arithmetic Comparison Circuits

Chapter 5: Flip-Flops, Registers and Counters

- 5.1 Basic Latch
- 5.2 Gated SR Latch
 - 5.2.1 Gated SR Latch with NAND Gates
- 5.3 Gated D Latch
 - 5.3.1 Effects of Propagation Delays
- 5.4 Edge-Triggered D Flip-Flops
 - 5.4.1 Master-Slave D Flip-Flop
 - 5.4.2 Other types of Edge-Triggered D Flip-Flops
 - 5.4.3 D Flip-Flops with Clear and Preset
- 5.5 T Flip-Flop
- 5.6 JK Flip-Flop
- 5.8 Registers
 - 5.8.1 Shift Register
 - 5.8.2 Parallel-Access Shift Register
- 5.9 Counters
 - 5.9.1 Asynchronous Counters
 - 5.9.2 Synchronous Counters
 - 5.9.3 Counters with Parallel Load

- 5.10 Reset Synchronization
- 5.11 Other Types of Counters
 - 5.11.1 BCD Counter
 - 5.11.2 Ring Counter
 - 5.11.3 Johnson Counter
- 5.14 Design Example
 - 5.14.1 Reaction Timer

Chapter 6: Synchronous Sequential Circuits

- 6.1 Basic Design Steps
 - 6.1.1 State Diagram
 - 6.1.2 State Table
 - 6.1.3 State Assignment
 - 6.1.4 Choice of Flip-Flops and Derivation of Next State and Output Expressions
 - 6.1.5 Timing Diagram
 - 6.1.6 Summary of Design Steps
- Example 6.1
- 6.2 State Assignment Problem
 - Example 6.2
 - 6.2.1 One Hot Encoding
- Example 6.3
- 6.3 Mealy State Model
 - Example 6.4
- 6.10 Algorithmic State Machine Chart

Chapter 7: Digital System Design

- 7.1 Bus Structure
 - 7.1.1 Using Tri-State Drivers to Implement a Bus
 - 7.1.2 Using Multiplexers to Implement a Bus
- 7.2 Simple Processor

Appendix B: Implementation Technology

- B.1 Transistor Switches
- B.2 NMOS Logic Gates
- B.3 CMOS Logic Gates
 - B.3.1 Speed of Logic Gate Circuits
- B.4 Negative Logic System
- B.8.8 Transmission Gates
- B.8.9-part (page-791) Drivers
- B.8.10 Tri-state Drivers
- B.9 Static Random Access Memory (SRAM)
 - B.9.1 SRAM Blocks in PLDs

Text Book:

Integrated Electronics: Analog and Digital Circuits and Systems, 2nd ed, - Jacob Millman, Christos Halkias and Chetan D Parikh

- 17.19 Digital-to-Analog Converters
- 17.20 Analog-to-Digital Converter