$-V_{DD}$ since device $Q1$ is OFF. The state of the storage cell is thus determined by detecting on which bit line the sense current flows.

To write 1 into the cell, the address lines are again pulsed and the ONE-bit line is grounded. Since the ONE-bit line is pulsed from $-V_{DD}$ to ground, this is interpreted to mean that we desire to write a 1 in the cell. However, the cell is already in the state to which it was to be written, and no change occurs because $Q2$ is already ON. If the ZERO-bit line is pulsed by grounding it, node N1 is pulled toward ground, turning device $Q2$ OFF and device $Q1$ ON through the regenerative process of the FLIP-FLOP. Thus the cell changes state, and we have written the logic 0 into the FLIP-FLOP. We observe that the reading process is nondestructive.

Typical cycle times for fully decoded bit-organized MOS chips generally lie in the range 500 ns to 1 μs. An example of a static MOS RAM is the MK 4002P (Mostek, Inc.). The unit is a 256-bit RAM, organized as 64 words of 4 bits each. It is TTL/DTL compatible because it uses low-threshhold p-channel MOS devices. Address decoding is performed on the chip from a binary 6-bit address which specifies each 4-bit word. The power supplies required are +5 and −12 V, and the device is available in a 24-pin dual-in-line package.

Dynamic MOS RAM[17] Instead of using an eight-device cell, it is possible to use a simpler three-device storage cell in which information is stored on the parasitic gate-to-substrate capacitance. Thus, at the expense of requiring a refresh operation to replenish the charge leaking off the storing capacitance, we achieve far greater density of storage cells on the same chip area.

An example of a dynamic MOS/LSI RAM is the 1103 manufactured by Intel Corp. This 1,024-bit memory is fully decoded and is organized as a 1,024-word by 1-bit array. Refreshing of all bits is required every 2 ms, and cycle time is 580 ns. The device is available in an 18-pin dual-in-line package. Power dissipation at room temperature is 400 mW.

IV. D/A AND A/D SYSTEMS

17-19 DIGITAL-TO-ANALOG CONVERTERS[19]

Many systems accept a digital word as an input signal and translate or convert it to an analog voltage or current. These systems are called *digital-to-analog*, or *D/A, converters*. The digital word is presented in a variety of codes, the most common being pure binary or binary-coded-decimal (BCD).

The output V_o of an N-bit D/A converter is given by the following equation:

$$V_o = (a_{N-1}2^{-1} + a_{N-2}2^{-2} + a_{N-3}2^{-3} + \cdots + a_0 2^{-N})V_R \qquad (17\text{-}33)$$

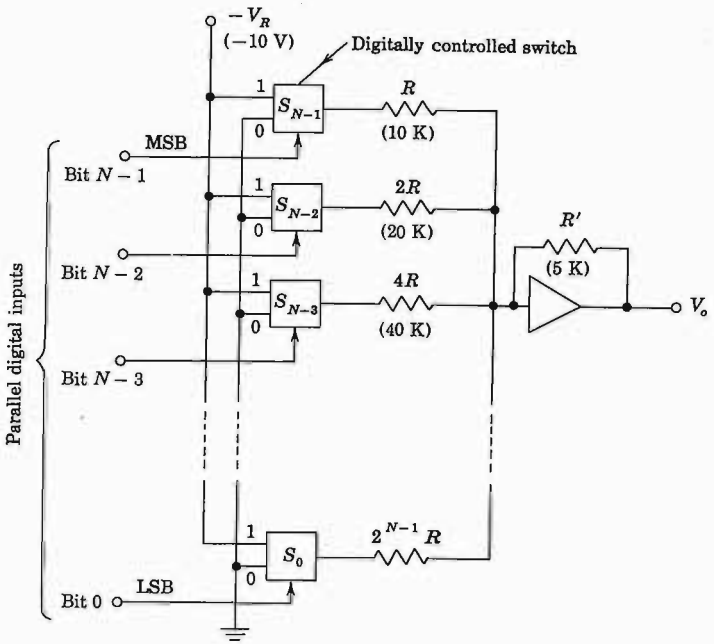


Fig. 17-58 D/A converter with binary weighted resistors.

where the coefficients a_n represent the binary word and $a_n = 1(0)$ if the nth bit is 1(0). The voltage V_R is a stable reference voltage used in the circuit. The most significant bit (MSB) is that corresponding to a_{N-1}, and its weight is $V_R/2$, while the least significant bit (LSB) corresponds to a_0, and its weight is $V_R/2^N$.

Consider, for example, a 5-bit word ($N = 5$) so that Eq. (17-33) becomes

$$V_o = (16a_4 + 8a_3 + 4a_2 + 2a_1 + a_0) \times \frac{V_R}{32} \tag{17-34}$$

For simplicity, assume $V_R = 32$ V. Then, if $a_0 = 1$ and all other a's are zero, we have $V_o = 1$. If $a_1 = 1$ and all other a's are zero, we obtain $V_o = 2$. If $a_0 = a_1 = 1$ and all other a's are zero, $V_o = 2 + 1 = 3$ V, etc. Clearly, V_o is an analog voltage proportional to the digital input.

A D/A converter is indicated schematically in Fig. 17-58. The blocks $S_0, S_1, S_2, \ldots, S_{N-1}$ in Fig. 17-58 are electronic switches which are digitally controlled. For example, when a 1 is present on the MSB line, switch S_{N-1} connects the 10-K resistor to the reference voltage $-V_R(-10$ V); conversely, when a 0 is present on the MSB line, the switch connects the resistor to the ground line. Thus the switch is a single-pole double-throw (SPDT) electronic switch. The operational amplifier acts as a current-to-voltage converter

(Sec. 16-1). Using the numerical values shown in Fig. 17-58, we see that if the MSB is 1 and all other bits are 0, then the current through the 10-K resistor will be 1 mA and the output voltage will be $V_o = 5 = 16 \times \frac{5}{16}$ V. Similarly, we see that the weight of the LSB (if $N = 5$) becomes $V_o = \frac{10}{160} \times 5 = 1 \times \frac{5}{16}$ V. If all five bits are 1, the output becomes

$$V_o = (1 + \tfrac{1}{2} + \tfrac{1}{4} + \tfrac{1}{8} + \tfrac{1}{16}) \times 5 = 31 \times \tfrac{5}{16}$$

Therefore the analog output V_o is proportional to the digital input; the proportionality factor is $\frac{5}{16}$ for the circuit of Fig. 17-58.

The implementation of the switching devices using p-channel MOS transistors is shown in Fig. 17-59. The S-R FLIP-FLOP is also implemented with MOSFETs and holds the bit on the corresponding bit line. Let us assume that logic 1 corresponds to -10 V and logic 0 corresponds to 0 V (negative logic). A 1 on the bit line sets the FLIP-FLOP at $Q = 1$ and $\bar{Q} = 0$, and thus transistor $Q1$ is ON, connecting the resistor R_1 to the reference voltage $-V_R$, while transistor $Q2$ is kept OFF. Similarly, a 0 at the input bit line will connect the resistor to the ground terminal. The accuracy and stability of this D/A converter depend primarily on the absolute accuracy of the resistors and the tracking of each other with temperature. Since all resistors are different and the largest is $2^{N-1}R$, where R is the smallest resistor, their values become excessively large, and it is very difficult and expensive to obtain stable, precise resistors of such values.

A Ladder-type D/A Converter A circuit utilizing twice the number of resistors in Fig. 17-58 for the same number of bits (N) but of values R and $2R$

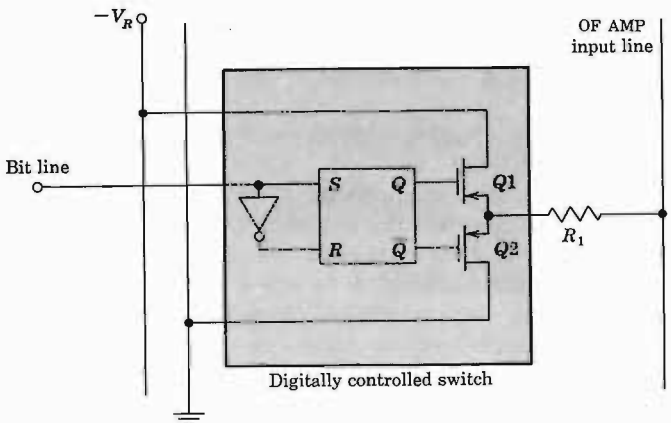


Fig. 17-59 An MOS FLIP-FLOP and a pair of MOSFETs implement the single-pole double-throw switch of Fig. 17-58. The resistance R_1 depends upon the bit under consideration. For example for the $N - 3$ bit, $R_1 = 4R$ (Fig. 17-58).

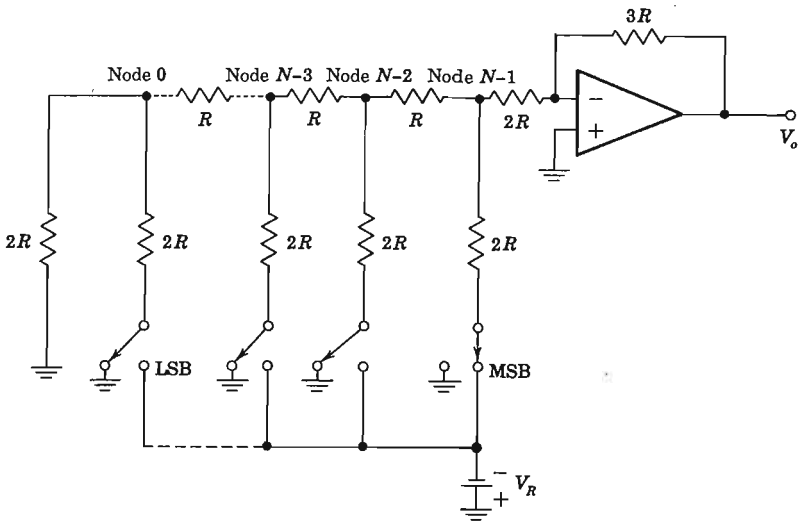


Fig. 17-60 D-to-A converter using R, $2R$ ladder.

only is shown in Fig. 17-60. The ladder used in this circuit is a current-splitting device, and thus the ratio of the resistors is more critical than their absolute value. We observe from the figure that at any of the ladder nodes the resistance is $2R$ looking to the left or the right or toward the switch. Hence the current will split equally toward the left and right, and this happens at every node. Considering node $N - 1$ and assuming the MSB turned ON, the voltage at that node will be $-V_R/3$. Since the gain of the operational amplifier to node $N - 1$ is $-3R/2R$, the weight of the MSB becomes

$$V_o = (-V_R/3)(-3R/2R) = V_R/2$$

Similarly, we show in Prob. 17-54 that when the second MSB bit is ON and all others are OFF, the output will be $V_o = +V_R/4$, the third MSB bit gives $+V_R/8$, and the LSB gives $+V_R/2^N$.

The circuits discussed so far use a negative reference voltage and give a positive analog output voltage. If negative binary numbers are to be converted, the sign-magnitude approach is used; an extra bit is added to the binary word to represent the sign, and this bit can be used to select the polarity of the reference voltage.

A typical 8-bit D/A converter by Zeltex Inc. is packaged in a module measuring 1.9 by 1.7 by 0.4 in. and includes the OP AMP, reference voltage, ladder network, and the switches. The 3750 D/A Converter (Fairchild Semiconductor) is a MOS/LSI 10-bit circuit using p-channel enhancement-mode transistors. The digital word can be entered serially or in parallel, and the

output is available through 10 SPDT MOS switches. The user must provide the resistive ladder network which is connected to the poles of the 10 switches. The 3750 contains an input shift register in which the data are stored and a holding register which retains the state of the previous 10-bit input word and drives the output switches. The device is available in a 36-pin dual-in-line package.

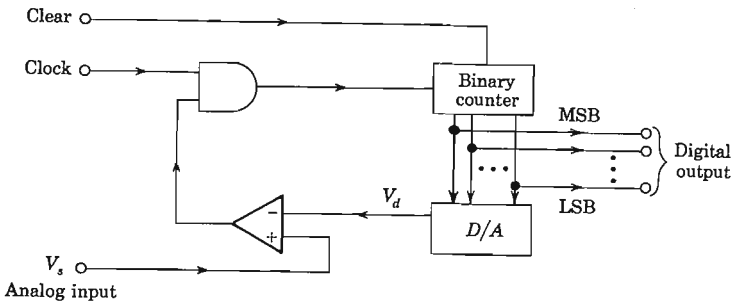
Multiplying D/A Converter A D/A converter which uses a varying analog signal instead of a fixed reference voltage is called a *multiplying D/A converter*. From Eq. (17-34) we see that the output is the product of the digital word and the analog voltage V_R and its value depends on the binary word (which represents a number smaller than unity). This arrangement is often referred to as a *programmable attenuator* because the output V_o is a fraction of the input V_R and the attenuator setting can be controlled by a computer.

17-20 ANALOG-TO-DIGITAL CONVERTER[19]

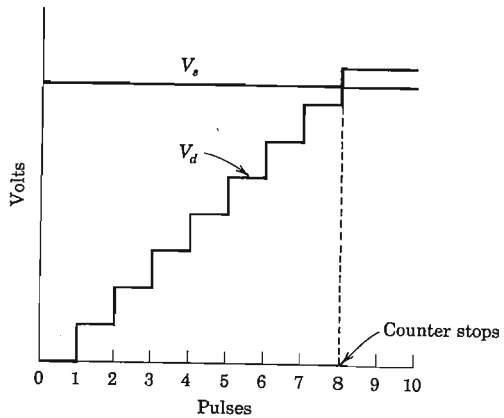
It is often required that data taken in a physical system be converted into digital form. Such data would normally appear in electrical analog form. For example, a temperature difference would be represented by the output of a thermocouple, the strain of a mechanical member would be represented by the electrical unbalance of a strain-gauge bridge, etc. The need therefore arises for a device that converts analog information into digital form. A very large number of such devices have been invented. We shall consider below one such A/D converter.

In this system a continuous sequence of equally spaced pulses is passed through a gate. The gate is normally closed, and is opened at the instant of the beginning of a linear ramp. The gate remains open until the linear sweep voltage attains the reference voltage of a comparator, the level of which is set equal to the analog voltage to be converted. The number of pulses in the train that pass through the gate is therefore proportional to the analog voltage. If the analog voltage varies with time, it will of course not be possible to convert the analog data continuously, but it will be required that the analog data be sampled at intervals. The maximum value of the analog voltage will be represented by a number of pulses n. It is clear that n should be made as large as possible consistent with the requirement that the time interval between two successive pulses shall be larger than the timing error of the time modulator. The recurrence frequency of the pulses is equal, at a minimum, to the product of n and the sampling rate. Actually, the recurrence rate will be larger in order to allow time for the circuit to recover between samplings.

One form of digital voltmeter uses the above-described analog-to-digital converter. The number of pulses which pass through the gate is proportional to the voltage being measured. These pulses go to a counter whose reading is



(a)



(b)

Fig. 17-61 (a) A/D converter using a counter; (b) counter ramp waveform.

indicated visually by means of some form of luminous display (Secs. 17-8 and 17-21).

The principles discussed previously are used in the A/D converter shown in Fig. 17-61*a*. The *clear* pulse resets the counter to the zero count. The counter then records in binary form the number of pulses from the clock line. The clock is a source of pulses equally spaced in time. Since the number of pulses counted increases linearly with time, the binary word representing this count is used as the input of a D/A converter whose output is shown in Fig. 17-61*b*. As long as the analog input V_s is greater than V_d, the comparator output is high and the AND gate is open for the transmission of the clock pulses to the counter. When V_d exceeds V_s, the comparator output changes to the low value, and the AND gate is disabled. This stops the counting at the time when $V_s \approx V_d$ and the counter can be read out as the digital word representing the analog input voltage.

Successive-approximation A/D Converter[19] The successive-approximation technique is another method to implement an A/D converter. Instead of a binary counter as shown in Fig. 17-61*a*, a programmer is used. The programmer sets the most significant bit (MSB) to 1, with all other bits to 0, and the comparator compares the D/A output with the analog signal. If the D/A output is larger, the 1 is removed from the MSB, and it is tried in the next most significant bit. If the analog input is larger, the 1 remains in that bit. Thus a 1 is tried in each bit of the D/A decoder until, at the end of the process, the binary equivalent of the analog signal is obtained. The 3751 MOS/LSI circuit (Fairchild Semiconductor) is a 12-bit A/D converter monolithic circuit which makes use of the successive-approximation technique. The ladder network must be supplied externally, and by choosing the appropriate coding of the resistor values in the ladder, the output can be in either binary or BCD digital form. The device is available in a 36-pin dual-in-line package.

17-21 CHARACTER GENERATORS[20,21]

This chapter concludes with a discussion of a two-dimensional alphanumeric character generation and display system. Many of the basic building blocks introduced in the preceding sections are involved in this fairly complicated system. For example, included are an ROM, a decoder, a parallel-to-series shift register, D/A converters, divide-by-N counters, and circulating shift-register memories.

The convenient display of information is a most important part of many electronic systems. Computers, calculators, business information systems, and similar systems commonly display information using alphanumeric characters on a cathode-ray tube (CRT), on seven-segment readouts, on indicator tubes, on lamp arrays, or as "hard copy" from matrix-type printers, etc. In many of these display applications, characters are generated using ROMs and long shift registers. MOS read-only memories offer a versatile approach to character generation because the ease of programming allows the designer to choose the characters and formats he desires.

Dot Matrix of a Character There are many character formats that can be designed into ROM character generators. The 5×7 dot-matrix format is easy to use and appears in many display systems. Consider the letter E shown in the 5×7 dot matrix of Fig. 17-62*a*. If each of the dot positions corresponds to a source of light or a lamp, the solid dots in the letter E are lamps which are ON, and the open dots are OFF light sources. The OFF lamps correspond to logic 0 outputs from an ROM with a $5 \times 7 = 35$-bit output word, while the ON lamps correspond to logic 1. To store 64 alphanumeric characters and other symbols, one ROM requires $64 \times 7 \times 5 = 2{,}240$ bits of storage. Implemented with diodes or bipolar transistors, such a memory is bulky and expensive